University of Bahrain
College of Information technology
Department of Computer Engineering

Test (2)

Student Name	
I.D. No.	
Section	

Course Title: Digital Logic
Course number: ITCE 202
Semester: 1
Academic Year: 2009/2010
Duration : 1 hour
Date: 4th January 2010

Read the following before you start:
1. Write your name, ID and section number
2. Answer all questions.
3. Write your answers on the attached sheets only.

Question	Mark	Mark attained
1	15	
2	15	
3	15	
4	5	
Total	50	

Question [1]: [15 mark]

a. Realize the following Boolean function as a multi-level 2-input all NAND gate circuit.

$$f = ABE' + C'E' + BD'E' + GH$$

b. Realize Z using a minimum 3-level all NOR gate circuit.

$$Z(A, B, C, D) = A'B' + ABD + ACD$$

Question [2] : [15 mark]

a. Implement F1 and F2 using one decoder and NAND logic gates.

$$F_1 = A'B' + BC$$
$$F_2 = \sum m(0,1,5)$$

b. Implement F using 4-to-1 Multiplexer with minimum number of additional logic gates. Connect inputs **A** and **B** to the selection lines of the multiplexer.

$$F(A,B,C,D) = \sum M(0,2,5,7,8,9,10,11)$$

Question [3]: [15 mark]

a. Specify the size of a ROM (number of words and number of bits per words) that will accommodate the truth table for the following combinational circuit:

1. A binary multiplier that multiplies 3-bit number by 2-bit number.

2. An 8-bit binary adder.

3. Generating the square of a 3-bit number.

b. Design a 3-bit binary adder\subtractor using full adders and any necessary logic gates.

Question [4]: [5 marks]

Complete the following timing diagram for the following latch